Device for controlling display elements in a display element array e.g. LCD arrays, comprises separate control circuit to handle each one of multiple display element subarrays

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Abstract of **DE19950839**

Display elements (8) are arranged in lines and columns. A separate control circuit (6) handles each one of multiple subarrays (4) in an array of display elements formed as a line or a column by multiple subarrays. Each subarray is formed in a line or column by multiple display elements. A first linking structure links each control circuit to the display elements for an allocated subarray. An Independent claim is included for a method for producing a display device.

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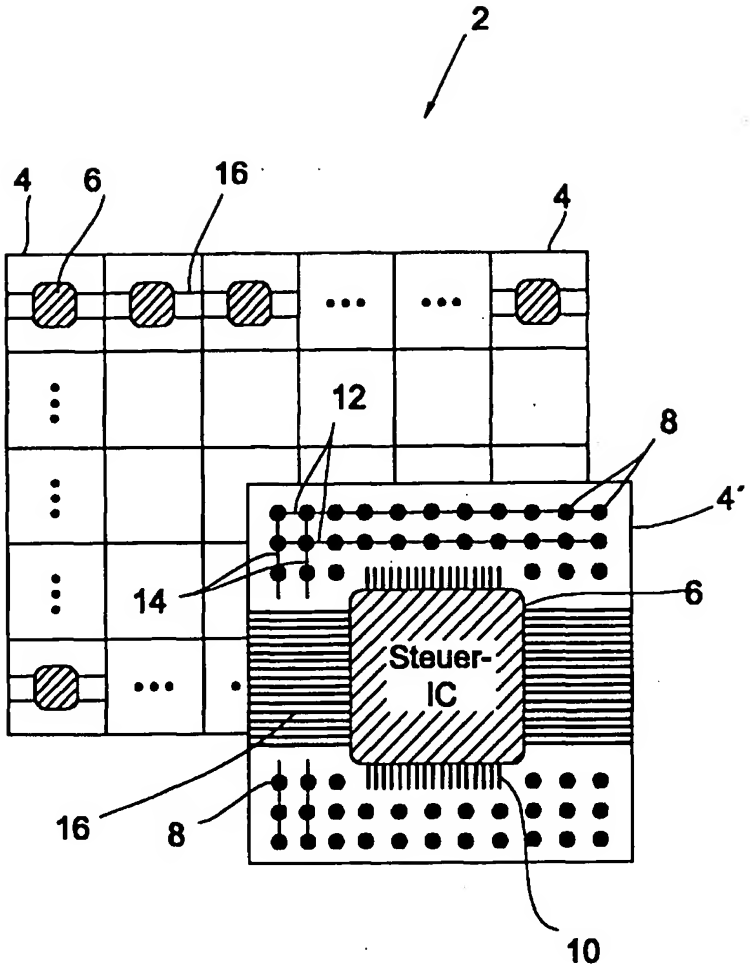

Fig. 1

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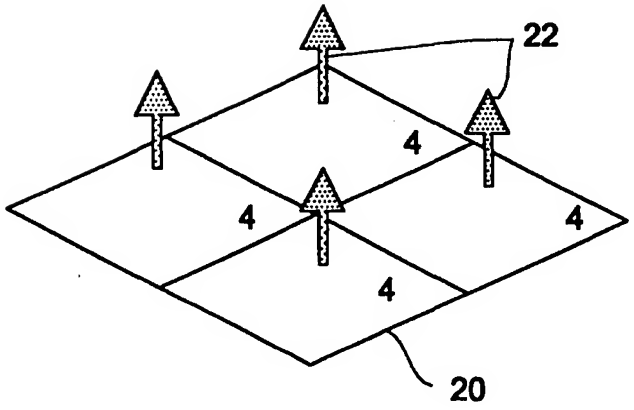

Fig. 2

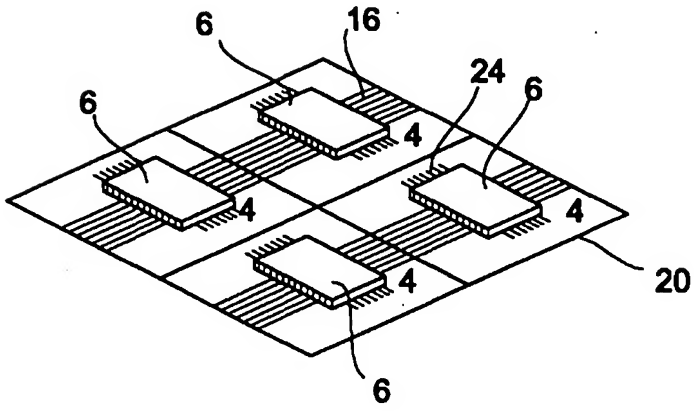

Fig. 3

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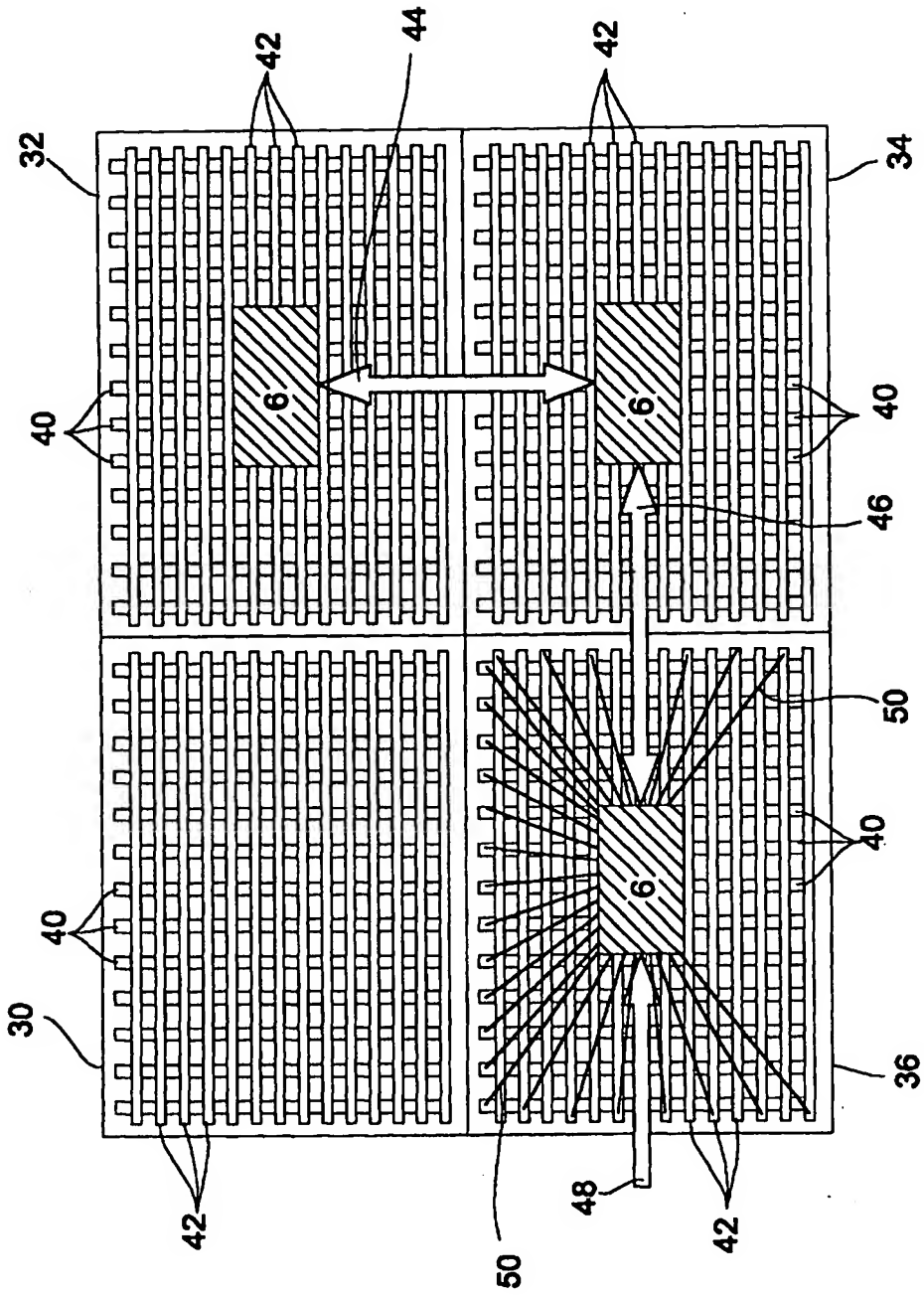

Fig. 4

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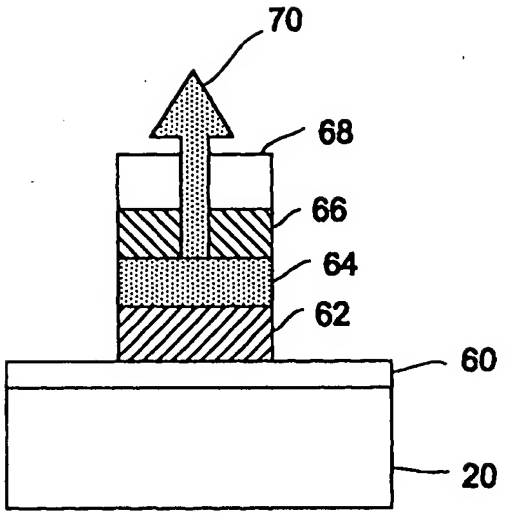

Fig. 5

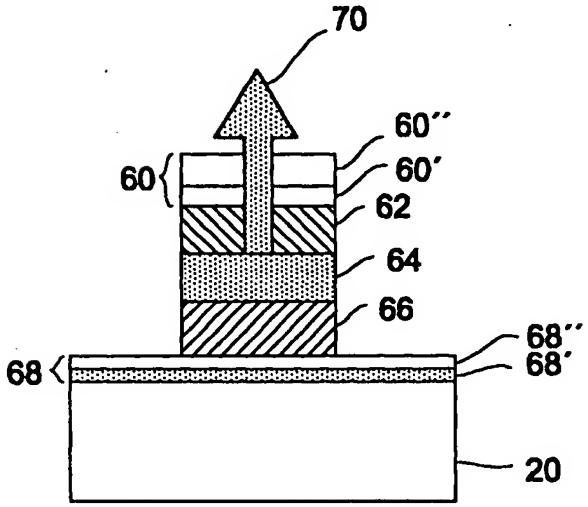

Fig. 6

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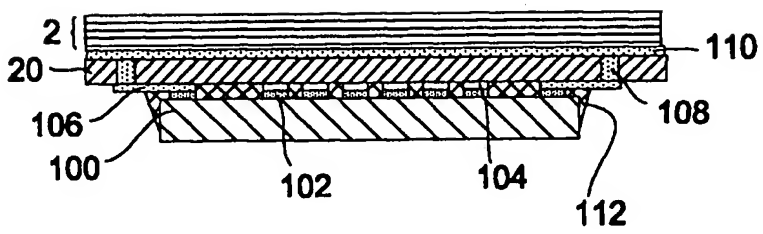

Fig. 7

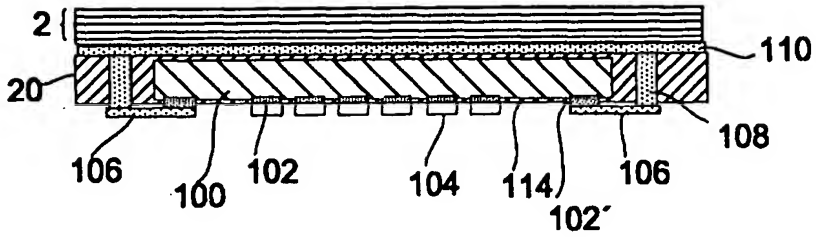

Fig. 8

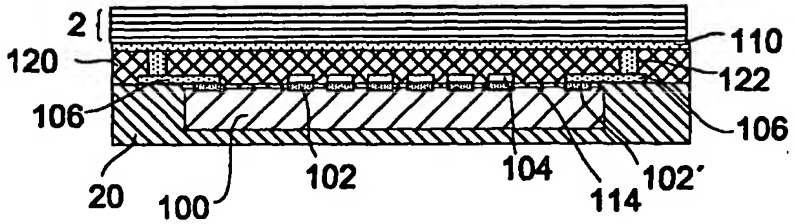

Fig. 9

Result Page

The available invention refers to a device for the control of the display elements of a display element array, which exhibits a multiplicity of display elements, which can be headed for, in order to use the display element array as indicator for computers and such a thing. The available invention refers furthermore to a procedure for manufacturing such a control device as well as the display element array.

To the control of so-called matrix displays, D. h. Arrays, which consist of a multiplicity of display elements, one of two well-known procedures is usually used at present. These well-known procedures are used in particular for the control of LCDs (LCD = liquid crystal display = liquid crystal display).

Hei small stencils and/or. small requirements of the indicator quality a passive matrix is used, which admits of lines/column multiplex cycle as so-called PM-LCD is and with that the display elements in is addressed. With applications with high order, how they are necessary with a laptop and such a thing for example, to a so-called active matrix control (AM-LCD) one falls back, which uses TFT electronics (TFT = thinfilm transistor = thin film transistor) using amorphouś or polycrystalline silicon on a glass base. This technology offers itself for LCD cells, since for the individual pixels of such LCD cells no control current is necessary, but only by a backup capacitor an electrical field to be kept upright must. Contrary to the above PM-technology the production of To-stencils is technologically complex, cost-intensive and with a high committee usually connected.

Beside the above LCDs arises in more recent time so-called oil since showing (OLED = Organic Light Emitting diode = organic light-along-animal-ends diode), which come on the market, whereby for such oil since showing still no established heading for techniques cut to it exist.

An organic lichtemittierendes element is for example in the U.S. - Described patent 5.834.893, whereby such an element from the following layer sequence is formed: Cathode, electron transport layer, light-along-animal-ends layer (elektrolumineszente layer), hole transport layer and anode. The electron transport layer, which elektrolumineszente layer and the hole transport layer consist of organic materials, whereby light-along-animal-end layer of organic elektrolumineszenten a material consists, which can become lively by an electric current, in order to emit light. With earlier ?classical? OLED structures the anode consisted of Indium tin oxide (ITO), which a transparent leader is, and was applied on a glass substrate, whereby the light emission took place by the anode and the glass substrate. The cathode consisted thereby of a layer of metal. On the other hand the U.S teaches. - Patent 5.834.893 an inverted OLED structure, with which the cathode is applied on a substrate, while the light emission takes place by the anode, which consists of Indium tin oxide, beabstandet arranged by the substrate. Regarding for OLEDs using materials is on revealing the U.S. - Referred patent 5.834.893.

The classical organic light emitting diodes described above are manufactured, as first a glass substrate is coated with Indium tin oxide as anode, whereupon the organic layer sequence, which of polymers or layers consist of small molecules, and finally the cover metallization, D. h. the cathode is separated. As mentioned, the light uncoupling takes place via the glass substrate, during with the inverted structure, those in the U.S with this structure. - Patent 5.834.893 described took place, the light uncoupling via the ITO anode.

Contrary to process card cells, which need light only to switch to have and therefore almost achievementless to be steered be able, OLEDs as if light-along-animal-end elements an electrical treasury rate. Further OLEDs are operated for the increase of the life span typically with a more complex tax cycle, with which the light achievement is stopped first by a Stromsteuerung in forward direction, while into the line tracing by a reverse voltage pulse interfacial traps in the organic materials are eliminated, whereby those can be drastically improved life lasting of the OLED elements.

Thus the realization of an active matrix control circuit with TFT electronics would exceed the complexity and thus the costs of oil since showing in relation to conventional To-controls for LCDs substantially, whereby besides the manufacturing yield would be clearly reduced. Over it also the use of a passive matrix is problematic for the control of oil since showing, since in the PM-mode the point light achievement of a line grows proportionally to the number of lines. With a number of 200 lines and a middle brightness of 200 cd/m< 2> for example a resulting pulse achievement of the line of 200 x 200 results cd/m< 2> = 40,000 cd/m< 2>. Here one pushes to the borders of OLED performance data, so that using the PM-mode announcements with small packing density can be only realized. Beyond that it is to be marked that the OLED dynamics permit not arbitrarily short tax cycles.

The task of the available invention consists of creating a economical device for the control of display elements in a display element array the one flexible control of the display elements also in complex display element arrays made possible.

This task is solved by a device in accordance with requirement 1.

A further task of the available invention consists of creating a procedure for the production of such a device.

This task is solved by a procedure in accordance with requirement 15.

The available invention creates a device for the control of the display elements of a display element array, whereby the display elements are arranged in lines and columns, with the following characteristics:
a separate gate circuit for everyone a majority by Unterarrays of the display element array, whereby the display element array is formed by Unterarrays at least either in line direction or in column direction by a majority, and whereby each Unterarray both in line direction and in column direction by a majority of display elements it is formed; and
a first connecting structure for connecting each gate circuit with the display elements of the assigned Unterarrays and a second connecting structure for connecting the separate gate circuits among themselves and/or with a superordinate gate circuit.

The available invention is based on the idea, an array and/or. a matrix of display elements into a majority of Unterarrays and/or. To partition Untermatrizen from display elements to, whereby a separate gate circuit is assigned to each Unterarray, so that the respective Unterarray can be steered either by a PM-control or by a To-control. Thus the available invention is suitable in particular for the control of oil since showing with high pixel number, for which a pure PM-control because of the necessary maximum performance and a pure To-control because of the TFT Schaltungskomplexität, in each case for the entire array, are not very promising. According to invention pixel driver electronics does not have to be arranged directly at the place of the respective pixel, as it is with to-technology the case. Rather driver electronics for a majority is summarized by pixels. Driver electronics and/or. Select electronics for a
▲ top respective group and/or. a respective Unterarray can be implemented for example as monolithically integrated silicon circuit. This silicon circuit for a respective Unterarray can then on the front using a dielectric cover and/or. the back using a plated-through hole of the substrate plate, on which the display element array is located, to be arranged.

Since the entire substrate surface for conductive strips structured for example lithographic, printed and such a thing, is it is available possible, for example in multilayer arrangements the individual pixels of the respective group directly to driver electronics of this group to be attached.

Alternatively it is possible, the pixels and/or. To head for display elements of a respective group in PM-multiplexing, D. h. using simple lines/column structure of parallel conductive strips. With this procedure the entire display area is arranged into small subranges, those parallel as Unterarrays and/or. Untermatrizen in multiplexing would work in each case. Thus a sufficient brightness of the announcement arises as a result of the heading for device according to invention also in the case of this simple procedure, since no more does not have to be operated the entire array in PM-multiplexing, so that the resulting pulse achievement depends not on the total volume of the display element array, but on the size of the respective Unterarrays. Thus know by those the available invention underlying idea to be in each case equipped wide display element arrays, for example oil since showing, while maintaining a sufficient indicator quality be operated same Unterarrays with separate gate circuits.

As mentions above, the available invention is suitable in particular for the control of oil since showing element arrays, and here in particular such oil since showing element arrays, with which the light uncoupling is made by the side of the OLEDs beabstandete by the carrier substrate. Thus the available invention is in particular for inverted OLED structures or suitable for OLED structures with transparent cathode. Thus heading for chips for whole lines and/or columns are not used according to invention, which are intended on an additional chip or an additional plate around the display element array on a carrier plate or. Rather in accordance with the available invention neighbouring display elements are combined both in line direction and in column direction into a Unterarray, whereby for each such Unterarray a separate gate circuit is intended. Thus all do not have in a column and/or in accordance with the available invention with the PM-mode. a line of arranged display elements by a gate circuit arranged at the edge to be headed for, but it can rather in each direction, D. h. in line direction and in column direction, a certain number of display elements to be selected, which is headed for by a common gate circuit. Depending upon desired quality thereby the Unterarrays can exhibit a smaller or larger number of display elements.

Before a procedure for manufacturing such a control device first a carrier substrate is made available, whereupon the gate circuits are implemented in or on a surface of the carrier substrate. After the implementation of the gate circuits the display element array on the surface of the carrier substrate, on which the gate circuits are implemented, or on this surface facing the surface produces.

The gate circuits can be thereby integrated circuits in lived form, which over SMT techniques (SMT = Surface Mount Technology = surface assembly technology) or sticking procedures are installed using anisotropic electrically conductive adhesives on the substrate back. Alternatively integrated circuits in unpackaged form can be used as gate circuits, which are attached by Flip chip procedures on the substrate back. Alternatively the chips with the inactive surface can be attached to the carrier substrate, whereby then an electrical connection can take place via wire bonding or a ISO-planar contacting. Again alternatively unpackaged integrated circuits can be used on the side of the carrier substrate as gate circuits, on which the display element array is then formed. For this purpose a ISO-planar contacting of the gate circuits is preferably used, whereby for it it must be only provided that over the gate circuits a planar surface is present, on which appropriate conductive strips and display elements be formed can.

The available invention creates thus a favourable device for the control of display elements of a display element matrix, which is suitable also for the control of wide display element arrays without quality loss. The available invention creates a display element array with respective gate circuits for Unterarrays of the same, whereby the display element array and the gate circuits are located on the same carrier substrate preferably. The individual gate circuits can be tested thereby before the final assembly separately, which leads to a cost reduction and an increase of the manufacturing yield.

Preferential training further of the available invention are stated in the dependent requirements.

Preferential remark examples of the available invention are more near described in the following referring to the enclosed designs. Show:

Fig. 1 a schematic representation for the illustration the heading for device according to invention of the underlying concept;

Fig. 2 and 3 schematic representations of the front and/or. the back of a remark example of an indicator according to invention;

Fig. 4 a schematic representation for the explanation of a remark example of a heading for device according to invention;

Fig. 5 and 6 schematic cross section opinions of remark examples of OLED elements; and

Fig. 7 to 9 schematic cross section opinions from remark different versions to the mounting of the gate circuits according to invention at the carrier substrate.

In the following preferential remark examples of the available invention are more near described referring to oil since showing. It is however here pointed out that the device according to invention can be used for the control of the display elements of a display element array also for other display element arrays, for example LCD arrays. With the preferential remark examples of the available invention it is only necessary that the light uncoupling takes place in each case in the direction, which faces the carrier substrate, so that the gate circuits on the carrier substrate, within the range of the Unterarrays, can be preferably arranged the respective gate circuit is assigned to which. This can be realized with LCD arrays by use of suitable reflectors.

A schematic representation for the illustration of the concept according to invention is in Fig. 1 shown, in the one display element array 2 into a majority of Unterarrays 4, with which represented remark example thirty, is partitioned. Each Unterarray 4 is provided with a controlling chip 6, which serves 8 of a respective Unterarrays for the control of the display elements, as by the increased representation 4 ' of a Unterarrays in Fig. 1 to see is. For this purpose the respective gate circuit 6 provided with connecting cables 10 is, by which a control of the individual display elements 8 can be accomplished either in form of a passive matrix control or in form of an active matrix control. In the increased section 4 ' only exemplarily two line feeder lines 12 as well as two column feeder lines 14 are represented, whereby it is however clear that for example for a PM-control all display elements of a Unterarrays are linemoderate and split-moderately connected. Furthermore is in Fig. 1 schematically a bus connection 16 shown, which can serve among themselves 6 for the connection of the gate circuits as well as for the connection the same with a superordinate control. Here the gate circuits of a line can be connected for example in each case. Alternatively also the gate circuits of a respective column can be connected. Again for example all gate circuits can exhibit a connection to each other in the bus connection 16.

Differently expressed the basic idea of the available invention consists of it, respective driver chips, D. h. Gate circuits, respective indicator under arrays, which can be called also indicator under stencils to assign. Preferably become thereby, as in Fig. 1 schematically shown is installed, the gate circuits within the surface of the individual indicator under array. As in the following referring to the Fig. to 7 to 9, can the gate circuits either on the front, D is more near described. h. the side, on which the display element array is developed, or on the back of the substrate plate to be applied.

A remark example, with which controlling chips 6 on the back of the carrier substrate are applied, is schematic in the Fig. 2 and 3 shown. Fig. 2 schematically the front of a carrier substrate 20, on which a display element array is formed, shows like schematically by four arrows 22, which are to represent radiated light, is indicated. Furthermore is schematic in Fig. 2 the partitioning of the display element array in four Unterarrays 4 represented. On the back of the carrier substrate 20 now a gate circuit 6 is intended, as in Fig for each Unterarray 4. 3 shown is. In Fig. 3 gate circuits shown can be circuits for example integrated in unpackaged form, which can be applied by means of a Flip chip technology on the back of the carrier substrate 20. Furthermore in Fig. 3 schematically represented is the conductive strips 16 for the heading for bus of the gate circuits 6. Beyond that the conductive strips 24 for the control of the display elements are schematic and/or. Pixels, which are located on the front of the carrier substrate 20, represented. These conductive strips 24 know for example by plated-through holes also on the front of the circuit substrate 20 arranged conductive strips (in Fig. 2) connected not shown its, as in the following referring to the Fig. one describes more near to 7 and 8.

Referring to Fig. 4 is more near described now the connecting structures of a heading for device according to invention for the realization of a passive matrix control. First it is marked that Fig. 4 four different ranges 30, 32, 34 and 36 shows, which are assigned to Unterarrays in each case. Its marked that in respective ranges not all connections are represented, but within some ranges for explanation purposes some the connections and/or. the gate circuit is omitted.

In the section 30 only the column lines 40 and line lines 42 necessary for the control of the individual display elements are shown. According to invention the column lines can be trained 40 for example as metallic lines, which form those for the carrier substrate of turned connections, while the line lines 42 can be trained for example made of Indium tin oxide, since these lines form the connections beabstandeten by the carrier substrate and thus in the light uncoupling way lie.

Furthermore in the section 32 the gate circuit 6, which is formed by an integrated silicon circuit preferably, is represented, which is connected by a bus, which is schematically by an arrow indicated to 44, with the gate circuit in the section 34. The gate circuit 6 in the section 34 is again connected by a bus, which is schematically by an arrow 46 shown, with a gate circuit 6 in the section 36. A further bus is schematically shown by an arrow 48, which can connect the gate circuit 6 in the section 36 with neighbouring gate circuits or with a superordinate external control. In this way the gate circuits can be connected in column direction among themselves, in line direction among themselves, in line and column direction among themselves and/or with a superordinate external gate circuit, which steers the full indicator reading of the display element array. Furthermore the Fig is in the section 36. 4 line and column addressing lines represented, by which two for example the reference symbol 50 is named. The line and column addressing lines are necessary, in order each individual display element, which is in each case at an intersection between column lines 40 and line lines 42, head for to be able. Here it is marked that the data buses 44, 46 and 48 as well as the lines/column address lines 50 can be preferably implemented by printings.

Alternatively to the described bus system for the external control of the gate circuits 6 led conductive strips can be intended also depending upon number of Unterarrays individually in each case to the gate circuits. The more Unterarrays, becomes the more favourable however the use of a bus system is intended.

Regarding the production for example in Fig. 2 and 3 represented remark example of a display element array with

assigned heading for device it is pointed out that preferably the structure of the individual function layers for the display element array takes place after the assembly of the gate circuits. Thus it is ensured that for example the function layers of the oil since showing elements are not destroyed by the assembly process of the gate circuits, for example the high process temperatures arising with it. For example temperatures of 220 DEG C are necessary when PbSn soldering necessary for installing the gate circuit. With the sequence for the production of the indicator, specified above, which is composed of a display element array and the control device according to invention, the possibility exists of using standard techniques for the assembly of the gate circuits which can exhibit also process parameters, which would damage otherwise the function layers of the oil since showing elements.

After now the heading for device according to invention was in detail described regarding the arrangement of the separate gate circuits as well as the connecting structures, in the following first with two OLED structures suitable for the available invention one deals, whereupon referring to the Fig. 7 to 9 remark examples for the attachment of the circuit chips on a carrier substrate, on which furthermore an oil since showing element array is located, to be described.

Fig. a schematic cross section opinion of a so-called shows 5 ?inverted? OLED. A cathode 60, which can consist for example of metal, located on the carrier substrate 20 is, which does not have to be due to the inverted structure of the OLED a glass substrate. On the cathode 60 are arranged for forming the inverted structure an electron transport layer 62 (ETL), a elektroluminеszente layer 64 (LEL), a hole transport layer 66 (HTL) and an anode 68, which consist of a transparent leader. The layers 62 to 66 consist of organic materials, whereby in the layer 44 the light 70 uncoupled over the anode is produced. Regarding the materials used for the individual layers is for example on revealing the U.S. - Patent referred 5.834.893, whereby the structure of OLED elements in the field of the technology admits is. Only referring to are mentioned that the anode 68 can consist of any transparent leader, for example Indium tin oxide, zinc oxide, copper oxide or a polymer, as long as the material for the light transparency produced in the layer 64 is. Furthermore a thin metallization layer can under the actual anode 68 (in Fig. 5) intended not shown its, which is likewise for the emitted light transparency.

Fig. a further example of an OLED element, which is suitable for the execution of the available invention, shows 6, whereby resembles elements as in Fig. 5 with same reference symbols is designated. Fig. no inverted structure shows 6, whereby the light uncoupling takes place here over the cathode 60, while the anode 68 on that is arranged the substrate 20 turned side of the OLED. As in Fig. 6 to see is, is formed the cathode 60 with the represented remark example from a thin layer of metal 60 ' and one over the thin layer of metal 60 ' arranged Indium tin oxide coating 60 ", which is both for the emitted light 70 transparency. Besides the anode 68 formed from a metallization layer 68 ' and one is on the same arranged Indium tin oxide coating 68 ", whereby the Indium tin oxide coating 68 " is intended here because of the electron affinity which can be overcome.

With the OLED structures described above the light 70 by the carrier substrate 20 is not uncoupled, so that the heading for device according to invention can be used here favourably, since those can be arranged the individual Unterarrays assigned heading for devices into the substrate 20 integrated or on the top side or lower surface of the same. Furthermore all necessary feeder lines can be arranged, without impairing the light uncoupling on the substrate 20. Examples of the assembly of controlling chips on the carrier substrate become in the following referring to the Fig. 7 to 9 describes.

In Fig. a schematic cross section representation of a remark example is shown 7, with which the gate circuit is formed by a unpackaged integrated circuit 100, which is arranged by means of a Flip chip connection on the back of the carrier substrate 20. With this so-called Flip chip connection the integrated circuit with the active side is installed to the substrate surface. Such a Flip chip connection can for example by a Flip chip Lötverfahren using an eutectic lead-tin-guides or through a sticking procedure using an anisotropic electrically conductive adhesive to be realized. In Fig. a remark example is represented 7, with which the integrated circuit 100 by means of a Flip chip Lötverfahrens at the carrier substrate 20 is appropriate.

For this purpose on the chip solder bumps 102 (so-called Lotbumps) are formed, as first a wettable Unterbumpmetallisierung is produced, for example by dead separating of nickel, whereupon on these Unterbumpmetallisierung the Lotbumps are produced. When assembling the IC chip 100 is placed in such a way that this Lotbumps 102 the contact areas of the carrier substrate 20, D. h. Conductive strips 104 and connection metallizations 106 of plated-through holes 108, opposite lie. The plated-through holes 108 are connected with conductive strips 110 on the chip 100 opposite surface of the carrier substrate 20. The conductive strips 110 represent for example the splitting and line lines for the individual display elements, those referring to Fig. 4 was described above. On the conductive strips the display element array 2 is for example referring in the form of an oil D-layer structure, like it to the Fig. 5 and 6 described one formed.

To applying the IC chip 100 on the back of the carrier substrate 20 it becomes returning after placing the IC chip 100, in such a manner that the Lotbumps 102 the contact areas 104, 106 of the carrier substrate 20 opposite to lie and/or. these affect, a thermal process accomplished, in order to melt the Lotbumps and to make a durable electrical connection between carrier chip 20 and chip 100. In order to cause a increased mechanical stability of the connection, the chip is under-filled preferably additionally with a hardening polymer 112.

Alternatively to referring above to Fig. 7 described soldering procedures can the chip also by means of an anisotropic electrically conductive adhesive at the carrier substrate 20 be attached, whereby then in place of guide the contact over the guidance particles of the adhesive, which are between the contact areas of chip and substrate, one realizes.

The described Flip chip procedure is suitable when using accordingly small and thin chips also for the structure of flexible indicators using thin, flexible circuit carriers.

Alternatively to the described Flip chip procedures the chips can also with the inactive surface, which chip back, to the carrier substrate are fastened, whereupon the electrical connection of the mating surfaces can be realized over a wire bonding.

An alternative procedure for the attachment of the circuit chip 100 on the back of the carrier substrate 20 is in Fig. 8 represented, whereby a ISO-planar contacting of the mating surfaces of the circuit chip takes place here. Here the circuit

chip must be very thin 100 and/or integrate in the substrate or an additional dielectric situation on the substrate. The dielectric situation can be produced thereby also after the assembly of the chip on the substrate and be opened in the places, in which electrical connections are to be implemented, again. With this procedure the chip is fastened with its inactive surface to the substrate.

As in Fig. , is brought in, in such a manner the circuit chip 100 is shown 8 into a cavity of the carrier substrate 20 that the active surface of the chip is essentially concise 100 with the lower surface of the carrier substrate 20. In order to arrange the circuit chip 100 in the carrier substrate 20, the same can be brought into a preformed recess in the carrier substrate 20, or be pressed over thermal processes into the substrate. If the chip is brought into the substrate, a passivation layer 114 on the chip 100 can be planned with exception of the chip contacts 102. Conductive strips 104, which at least partly are over the chip contacts 102, become following, and conductive strips 106, which connect outside chip contacts 102 ' with the throughholes 108 by the carrier substrate 20, produces. These conductive strips 104 and 106 can either in thin-film technology by galvanic or chemical metal separation or by laying on of conductive polymers, which are leading by filling particles leading or, which corresponds to a thick film technique, are produced. Again alternatively the conductive strips can be produced by adhesives by means of pressures, dispensations, stamps or other Transferverfahren. For this it is possibly necessary, the contact areas of the chip 102, 102 ' with a metallization, which resembles a Unterbumpmetallisierung, which protects the aluminum surface of the contact area of the chip and exhibits a good electrically leading surface, to provide. Also with this remark example a flexible indicator can be realized when using according to gedünnten, flexible chips 100 in connection with flexible carrier substrates 20.

Alternatively to the possibilities specified above of arranging unpackaged IC chips on the back of the carrier substrate 20 circuits in lived form, also integrated, can be installed for example by means of the SMT technology or by sticking procedures using an anisotropic electrically conductive adhesive on the substrate back. Possible housings for such ICs cover the so-called Quad Flat luggage, the Tape carrier Package, chip the Scale Package etc.

It is common to the procedures for the attachment of the chips on the back of the carrier substrate that the substrate contains the appropriate conductive strips and mating surfaces on the back, whereby these conductive strips and mating surfaces are connected by electrical plated-through holes to the front with the conductive strips on the front. On these conductive strips on the front of the carrier substrate 20 after installing the circuit chip the function layers of the indicator are developed.

In Fig. now an alternative remark example is represented 9, with that the circuit chip 100 in the front of the carrier substrate 20, D. h. in the surface, on which the OLED structures 2 are formed later, is produced. As shown, is the circuit chip is 100 again into a recess of the carrier substrate 20, which is however this time in the front of the carrier substrate 20, brought in, whereby over the chip 100 again a passivation layer is arranged. On the contacts 102 and 102 ' of the chip 100 is formed again for conductive strips 104 and 106. After forming the conductive strips with the represented remark example a dielectric layer 120 was produced, in order to create a planar surface. In the dielectric layer 120 or plated-through holes 122 are are planned, in order to realize a connection of the chip contacts 102 ' over the conductive strips 106 and the plated-through holes 122 with conductive strips 110. On the conductive strips 110 the function layers of the OLED structure 2 are produced in the following.

Referring above to Fig. a possibility for ISO-planar contacting represents 9 described example. Alternatively to bringing the chip into a cavity in the substrate the chip can be applied first on the substrate, whereupon a dielectric situation is produced after the assembly of the chip on the substrate and then in the appropriate places is again opened. Further alternatively it is possible to install very thin flexible chips on the substrate surface.

Alternatively to the structure described above can on applying an additional dielectric situation, the dielectric layer 120 in Fig. 9, over the chip and the substrate for the reconciliation of the unevenness to be done without, if the chip is finally integrated either flat with the substrate surface in the substrate or the Planarisierung with the first dielectric layer, which is formed as it were around the chip, taken place. In deviation to subsequent applying of the dielectric situation, in which the chip is arranged, the chip can be integrated when applying the same into a dielectric situation.

Also with the remark examples for the ISO-planar contacting of the gate circuits on the front the conductive strips can be produced in each case in thin-film technology or thick film technique. Furthermore gedünnte, flexible chips in connection with flexible circuit carriers can be used, so that the possibility of the realization of flexible indicators exists also here.

With the procedures for the production of an indicator, described above, a Unterarray of display elements always becomes a gate circuit on the back and/or for. Front of the carrier substrate applied. For example thirty if Unterarrays are intended, onto the described way thirty gate circuits are installed. The assembly of the gate circuits will was preferably accomplished, as above described, before applying the function layers of the OLED structures 2, in order to avoid a damage of the function layers by following processes. If no processes are necessary for the production of the gate circuits, which can impair the function layers, then the production of the function layers can take place also before the production of the gate circuits.

Finally it is again marked that into the Fig. 7 to 9 represented conductive strips 104 for example in Fig. 3 penalties shown 16 correspond, while the conductive strips 106 in Fig. 3 connecting cables shown 24 correspond, then over plated-through holes to the surface of the carrier substrate and/or. one on the same arranged dielectric layer to be led, over with the conductive strips 110, those for example in Fig. 4 column lines shown 40 and line lines 42 represent to be connected.

The available invention makes thus beside a favourable heading for device for picture element arrays the simple and economical realization possible of indicators, with which gate circuits for everyone a majority the connecting structures on a carrier substrate, necessary by Unterarrays as well as associated display elements and, are arranged.